INF4420 - PROJECTS IN ANALOGUE/MIXED-SIGNAL CMOS DESIGN

The design of a switched-capacitor S/H

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Abstract

Sample-and-hold (S/H) are a major part of analog to digital converters. This paper presents the design and layout of a switched-capacitor sample-and hold and low-pass filter, as well as a multiphase clock generator. The paper is meant as a learning experience in analogue/mixed-signal CMOS design.

1 Introduction

A sample-and-hold is used to sample an analog signal and store its value for a length of time. It is an important part of data-converter systems, and a necessary component in many data-acquisition systems such as A/D converters. The use of a S/H can greatly reduce errors due to slightly different time delays in the internal operation of the converter. Sample-and-holds are subject to several nonidealities characterized in terms of their hold step, input isolation, tracking bandwidth, slew rate, droop rate, and aperture uncertainty, in addition to usual analog performance metrics such as dynamic range, linearity, etc. Since we were given the schematics for the S/H our main problem was to properly size C_1 in order to achieve a SNR of 10bits, and to size the switches to get proper settling. We also had to determine the C_1 and C_2 ratio and the sampling frequency. The specifications of the S/H are as follows:

- input signal bandwidth: 1MHZ
- Input swing: 300 $\mathrm{mV_{pp}}$
- In-band attenuation: < 3 dB
- Input common mode voltage: 600 mV
- Dynamic range: > 8 bits
- Settling error: < 1%
- Cload: 200 fF

After finishing the schematic we swept the input frequency from 100 kHz to 1 MHz to find the in-band attenuation, and swept the magnitude of the input signal with $f_{in} = 100$ kHz estimating the dynamic range. The layout was done in a 90 nm CMOS process, and after wards the simulations were run on the layout and compared to the pre-layout simulation. The sample-and-hold preforms within the given specifications both pre- and post-layout.
The schematics and layouts files can be found in the directory:
"/uio/aristoteles/s10/maristal/cadence61_tsmc90nmlp_oa/mittlib/". The layout of the complete circuit is under "sh_clk".

Contents

2 Circuit implementation

Fig. 1 shows the schematic of our implementation of the slightly modified sample-and-hold circuit in [1, p.456]. We modified the design slightly by replacing two of the n-channel switches with CMOS transmission gates. This resulted in the effective R_{on} being lower, which in turn allowed us to use larger capacitors which met our switching noise requirement of a SNR of 10bits. The AC ground is connected to the positive input of the op amp, and the source of the nmos that is clocked with clk1'.

2.1 Capacitors sizing and design

We considered only the switching noise, therefore $V^2_{n(rms)} = \frac{kT}{c}$. $V_{x(rms)} = \frac{V_A^2}{2}$, where V_A is 150mV, assume the temperature T is 300 Kelvin, and k is the Boltzmann constant. The size of C1 in order to achieve a SNR of 10 bits was calculated using eq. 1.

$$\text{SNR} = 10 \log \left[\frac{V_{x(rms)}}{V^2_{n(rms)}} \right] = 62\,\text{dB} \tag{1}$$

$$10 \log x = 62\text{dB} \qquad \frac{V^2_{x(rms)}}{V^2_{n(rms)}} = x$$

$$\frac{62}{10} = \log x \qquad \frac{\frac{V_A^2}{2}}{\frac{kT}{C1}} = 1259^2$$

$$x = 10^{\frac{62}{10}} \qquad \frac{C1 V_A^2}{2kT} = x$$

$$x = 1584893.2 \qquad C1 = \frac{x \times 2kT}{V_A^2}$$

$$C1 = 583.5\,\text{fF}$$

When determining the ratio of C1 to C2 we considered equation 2. It tells us that if we were to use a very large C2, then we would need a high clock frequency to meet our bandwidth requirement. With a higher clock frequency we would need faster settling time, which could be achieved by increasing the width of the switches. However this would increase the charge injection because of the increased gate area. A high clock frequency would also require more power. We decided to make C2 1.33 times larger than C1, this would allow us to use a lower clock frequency. According to equation 2 we would only need a clock frequency of about 8MHz, however we choose to use a clock frequency of 25MHz as it is low enough to get good settling with our transistor sizing, and over sampling helps avoid aliasing. Note that equation 2 is only a valid approximation when C2 is at least a few times greater than C1 [1, p.455].

$$\text{f}_{-3\text{dB}} = \frac{C_1}{2\pi \text{C2}} \text{f}_{\text{clk}} \tag{2}$$

2.2 Capacitor layout

There are several sources of error to the absolute values of capacitors in integrated circuits, both systematic and random. It is easier to control the matching of the capacitors to get a

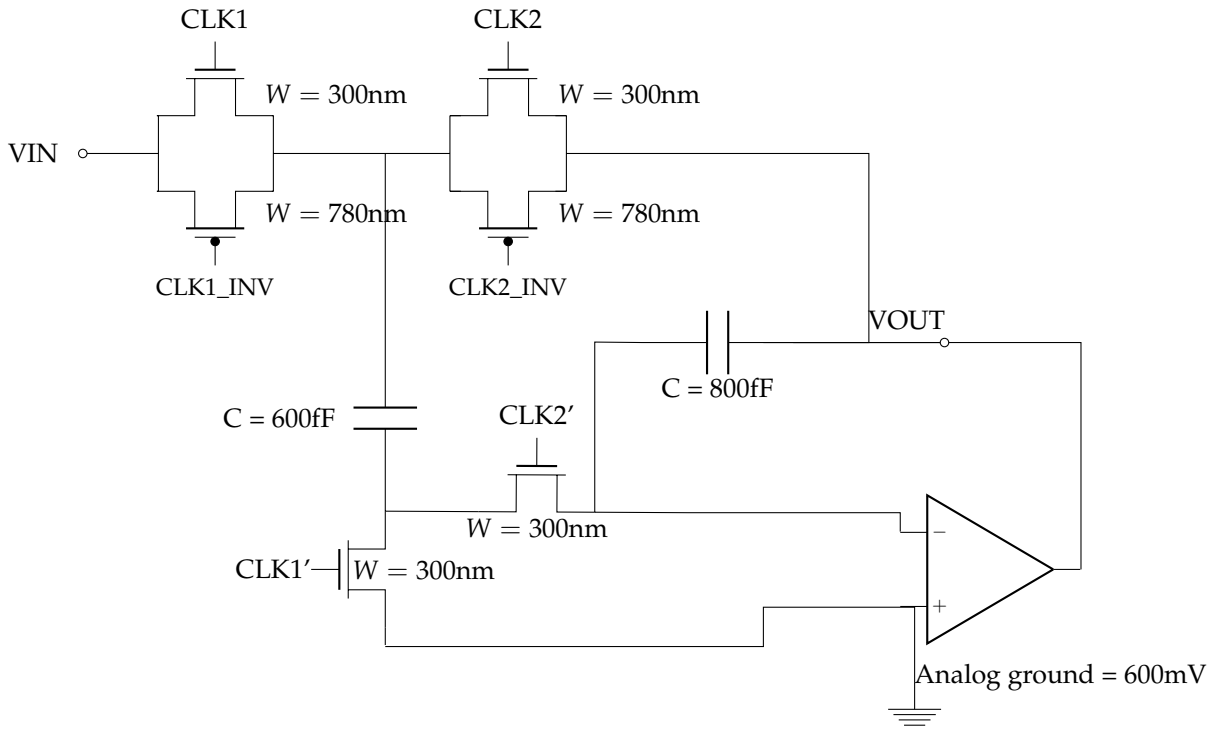


Figure 1: Schematic of the sample-and-hold showing sizes of components. All the transistors have minimum length = 100nm.

consistent ratio, than to control the absolute values. Therefore the circuit is designed so that the cutoff frequency is determined by the ratio of the capacitors (eq. 2). One way to get good matching is to use unit-sized capacitors in a common-centroid layout where each unit has the same surroundings. Common-centroid is used when critical matching is required, another way of doing it when you don't need perfect matching is interdigitated layout. Our design has a requirement of in-band attenuation < 3 dB for input signals of up to 1 MHz. We choose to use a higher clock frequency than necessary, according to eq. 2 this should give us a higher -3 dB point, which will allow for the the capacitor ratio to vary without moving the -3 dB point below 1 MHz. We therefore chose $C_1 = 600$ fF and $C_2 = 800$ fF. These could easily be realized with unit capacitors of size 200 fF, where C_1 needed three of the unit-sized capacitors in parallel and C_2 needed four. We realized the capacitors in the layout by using unit capacitors of size 200 µm, 3 units for C_1 and 4 units for C_2. The units were interspersed in an interdigitated layout, we felt it was unnecessary to use a common-centroid layout since it would be harder to realize and would need a larger area, and our design allows for some variance of the capacitor ratio since the chosen clock frequency is so high. It would have an effect on the bandwidth, which we already have a good margin on. In other words, we placed the units in a row starting with a C_2 unit then a C_1 unit, then a C_2 unit and so on. On each end we placed a grounded unit capacitor, so that all the working units had matching boundary conditions.

2.3 Switch design

The CMOS-switch on the input of the S/H and capacitor C1 can be modeled as a RC circuit where R is R_{on} and C is C1. The capacitor size is already chosen so we needed to find a suitable

R_{on} that will give a settling time of the RC circuit < 1%. This was accomplished using equation 3 where T_s is slightly less than $\frac{period}{2}$. When $f_{clk} = 25\,\text{MHz}$ we get $T_s = \frac{40\,\text{ns}}{2} \approx 20\,\text{ns}$ and $R = \frac{20\,\text{ns}}{C1 \times \log\left(\frac{1}{0.01}\right)} = 7.238\,\text{k}\Omega$

$$T_s = RC \log\left(\frac{1}{1\%}\right) \tag{3}$$

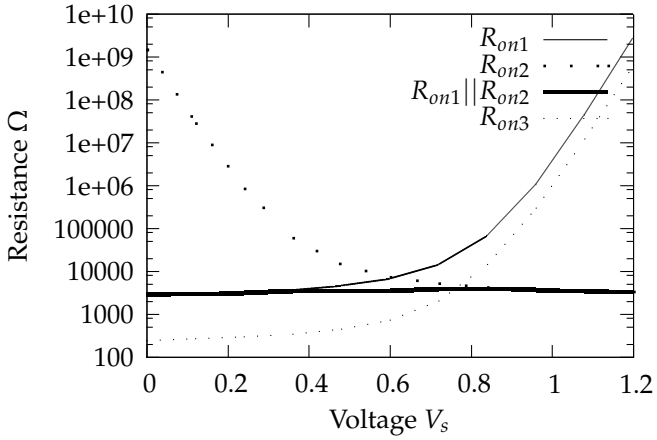


Figure 2: Nominal plot of the resistance in CMOS switch where R_{on1} is PMOS R_{on}, R_{on2} is NMOS R_{on} and R_{on3} is a single NMOS R_{on}. The parallel of R_{on1} and R_{on2} is also plotted.

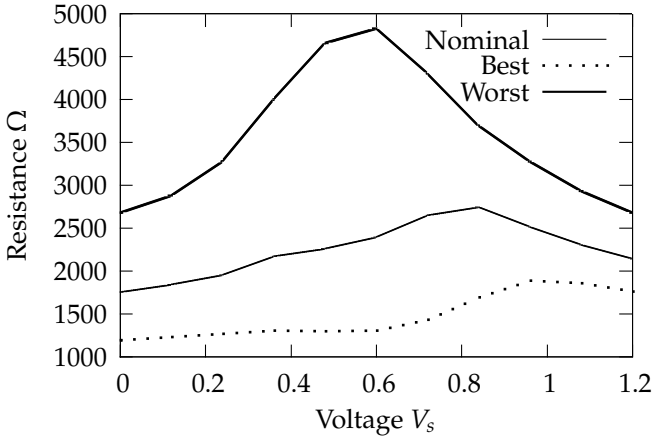


Figure 3: The parallel of R_{on1} and R_{on2} when NMOS width is 300 nm and PMOS width is 780 nm.

To get $R_{on} < 7.2\,\text{k}\Omega$, using a single NMOS as a switch was not enough. Using a NMOS and PMOS as a transmission gate the total R_{on} is the parallel of the R_{on} from the NMOS and PMOS. We chose the widths 300 nm for the NMOS and 780 nm for the PMOS. The results are shown in Fig. 2, with a closer look at the total R_{on} in Fig. 3. R_{on} is now lower than $5\,\text{k}\Omega$, in all the corners shown in Fig. 3. We chose the ratio $\frac{PMOSwidth}{NMOSwidth} = 2.6$ because of the reduced charge mobility of the PMOS. There is a trade off here, the switches will consume more power because of the wider p channel, however the circuit will settle faster when going from zero to one. The switches are larger than they needed to be, which could lead to larger charge injection. We could have made them smaller as long as R_{on} stays below $7.2\,\text{k}\Omega$, which would decrease the charge injection since it is proportional to the transistor size.

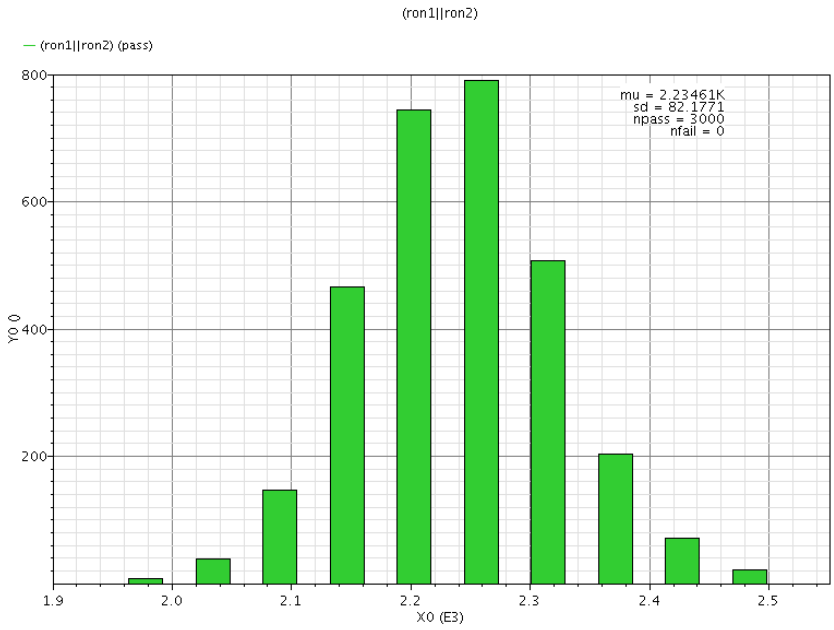


Figure 4: Montecarlo probability distribution of R_{on} in CMOS switch 3000 steps.

We also ran a montecarlo simulation to find a probability distribution of the resistance, seen in Fig. 4 and the settling time of C1 see Fig. 5. The problem with the montecarlo simulation, is that we were unable to sweep variables. The distribution has $\mu = 2235\Omega$ and $\sigma = 82.2$, then we get $2235 + 3 \times 82.2 = 2481.6\Omega$. This number is still lower than 7.2KΩ which was the upper limit. It is however lower than expected. This should not be a problem though since a smaller R_{on} should fill up the S/H capacitor faster, making it settle fast enough.

2.4 Settling time

To find the settling time we connected one of the switches to C_1 and looked at the step response, the schematic Fig. 10 can be seen in appendix A. The required settling time is the on-time of ϕ_1 which is 19.5ns, the allowed settling error is 1%. We then found the maximum step size as:

$$\int_0^{40n} sin(2\pi f_{max} x)dx = 2\pi f_{max} sin(2\pi f_{max}) = 2\pi 1\text{MHz}40\text{ns} = 251\text{mV} \tag{4}$$

We then ran a Monte Carlo simulation to find how much time it would take to settle to $< 1\%$ which is $99\%(600\text{mV} + 251\text{mV}) = 848\text{mV}$. We can see that the 3σ worst case settling time is $mean + 3 * standarddeviation = 13.95\text{ns}$ which meets the requirements.

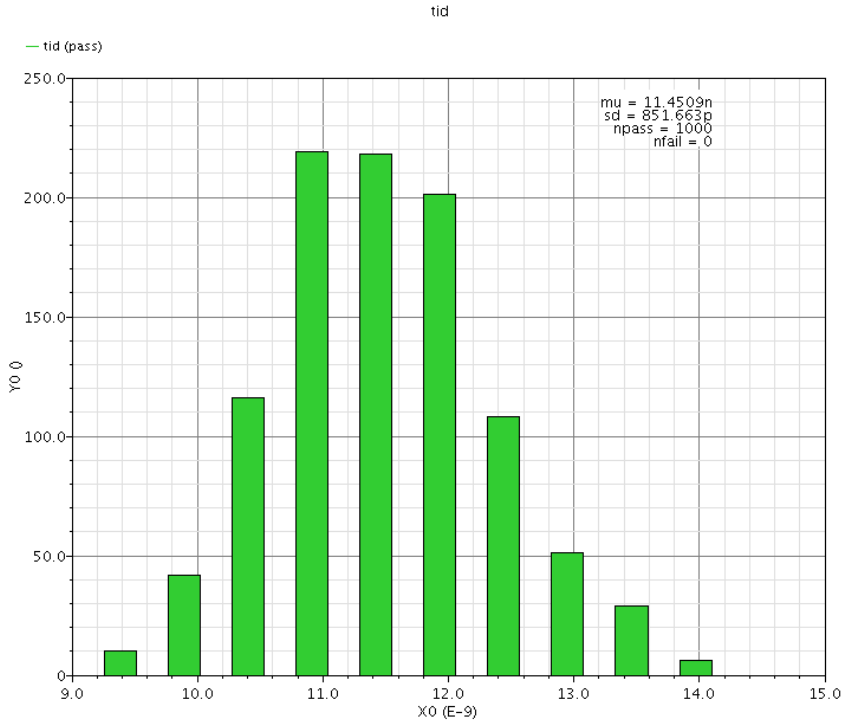


Figure 5: Montecarlo simulation of CMOS switch showing settling time.

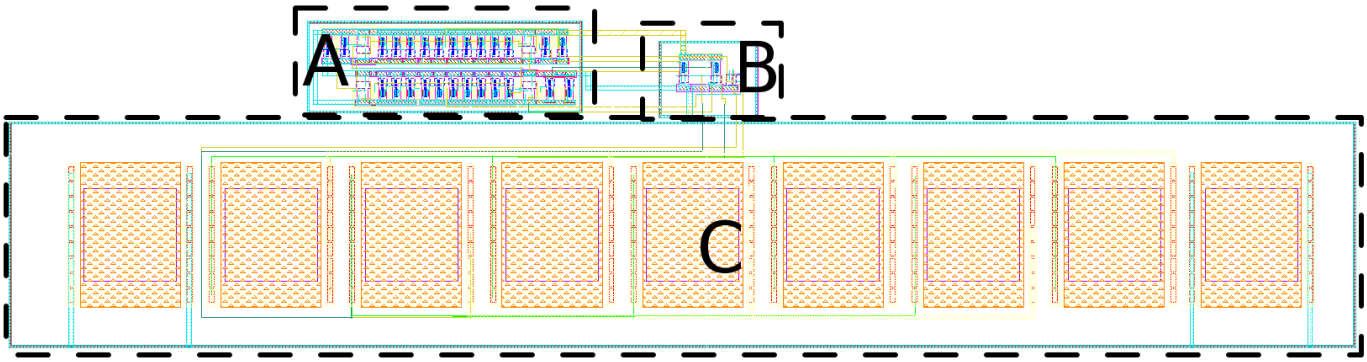


Figure 6: Circuit layout (A:clock generator; B: sample-and-hold; C: Capacitors)

2.5 Vias

When drawing the layout we chose to use vias with four connectors wherever possible. This will reduce the resistance in the connections since one via has about 10Ω resistance, it should also give a higher yield when producing the circuit because of redundancy.

2.6 Clock generator

The clock generator uses delay elements to create 8 different clocks, where ϕ_1 and ϕ_1' and ϕ_2 and ϕ_2' are phase shifted relative to each other. The delay in the clock phases is to reduce charge injection. With turning the clock ϕ_1' before ϕ_1 the capacitor C1 will see a great impedance from the transistor and most of the charge will flow out through the input, thus reducing the charge injection. The output of the clock generator can be seen in the appendix fig. 14 with the delay between clocks marked. For ϕ_1 and ϕ_1' the delay is 156ps or 0.8% of the clock period and for ϕ_2 and ϕ_2' or 0.3% of the clock period. The delay is good enough considering that adding delay elements and/or increasing their size would make the layout of the clock generator more complicated and bigger. A plot of the clock phases can be seen in fig. 14

2.7 Layout Area

Fig. 6 shows the circuit layout with the different parts marked. We placed a guard ring around each part; A, B and C. The guard rings increases the area slightly, however they are good at screening analog parts of the circuit from noise coming from digital circuits, which produce noise because of the fast switching. The switches which are clocked by clk1′ and clk2′ share a drain, this reduces the area and reduces parasitic capacitance C_{dg}. The total area is $34.5\,\mu\text{m} \times 142.5\,\mu\text{m} = 4.92\,\text{nm}$

3 Results

We swept the input frequency from 100kHz to 1.5 MHz with a step size of 100kHz, shown in fig. 7. The in-band attenuation is -2.150dB for post-layout and -2.099dB for pre-layout. The -3dB point is at 1.22MHz for both pre- and post-layout.

To estimate the dynamic range we first found the SNDR by sweeping the magnitude of the input signal with $f_{in} = 100kHz$ pre- and post-layout. The simulations were run for 120ms with noise parameters set as $f_{MAX} = 200\text{MHz}$, $f_{MIN} = 10\text{kHz}$. We then calculated the DFT with window type set to Hamming and with NFFT $= 4096$. We then calculated SNDR by finding the spectrum of the output signal using the equation 9.150 [1, p.404]
$\text{SNDR} = 10\log(\frac{V_f^2}{N_o+Vh2^2+V_{h3}^2+\cdots})$ The results are shown in Fig. 8. We can see that SNDR is most limited by distortion in the pre-layout and by distortion on post-layout. We then estimated the dynamic range using a matlab script (see appendix B), results shown in table below. The dynamic range for pre-layout is 8.03 bits and for post layout 8.74 bits.

To estimate the power usage of the circuit pre- and post-layout we simulated the circuit for one period and then calculated the rms value of the current used by the source times 1.2V.

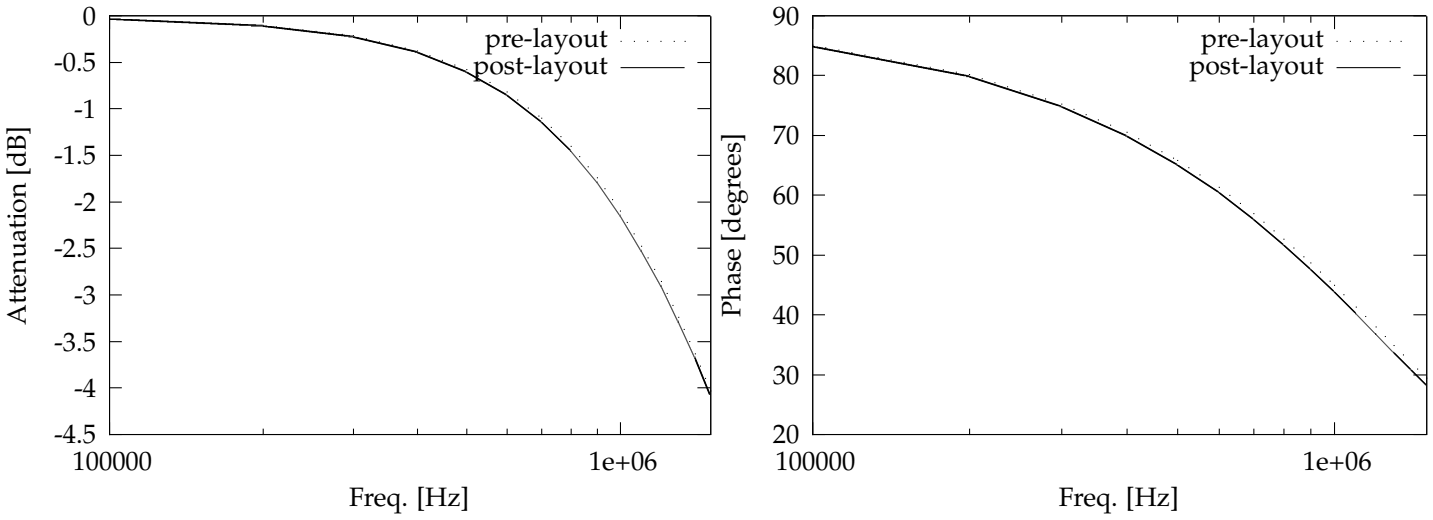
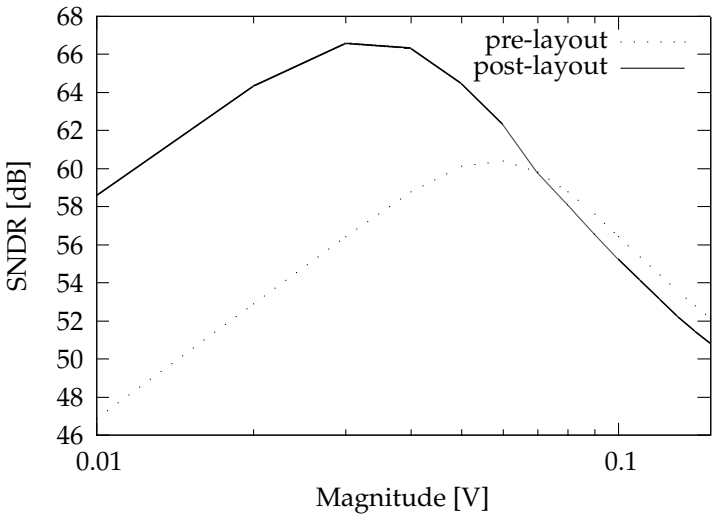


Figure 7: Frequency response for attenuation and phase pre- and post-layout.



Dynamic range pre- and post-layout

Magnitude [V]	pre-layout [bits]	post-layout [bits]
0.010	8.08	10.09
0.020	9.08	11.04
0.030	9.67	11.40
0.040	10.06	11.34
0.050	10.28	11.02
0.060	10.33	10.65
0.070	10.24	10.23
0.080	10.06	9.95
0.090	9.87	9.69
0.100	9.67	9.48
0.110	9.49	9.29
0.120	9.33	9.12
0.130	9.19	8.97
0.140	9.07	8.85
0.150	8.95	8.74

Figure 8: Input signal magnitude sweep from 10 to 150mV$_{\text{pp}}$ with $f_{in} = 100$kHz

4 Discussion

4.1 Capacitors

We realized later during the layout that we probably could have made C_2 twice the size of C_1, and made the unit-sized capacitor 600fF. Then we would only have needed one unit-sized

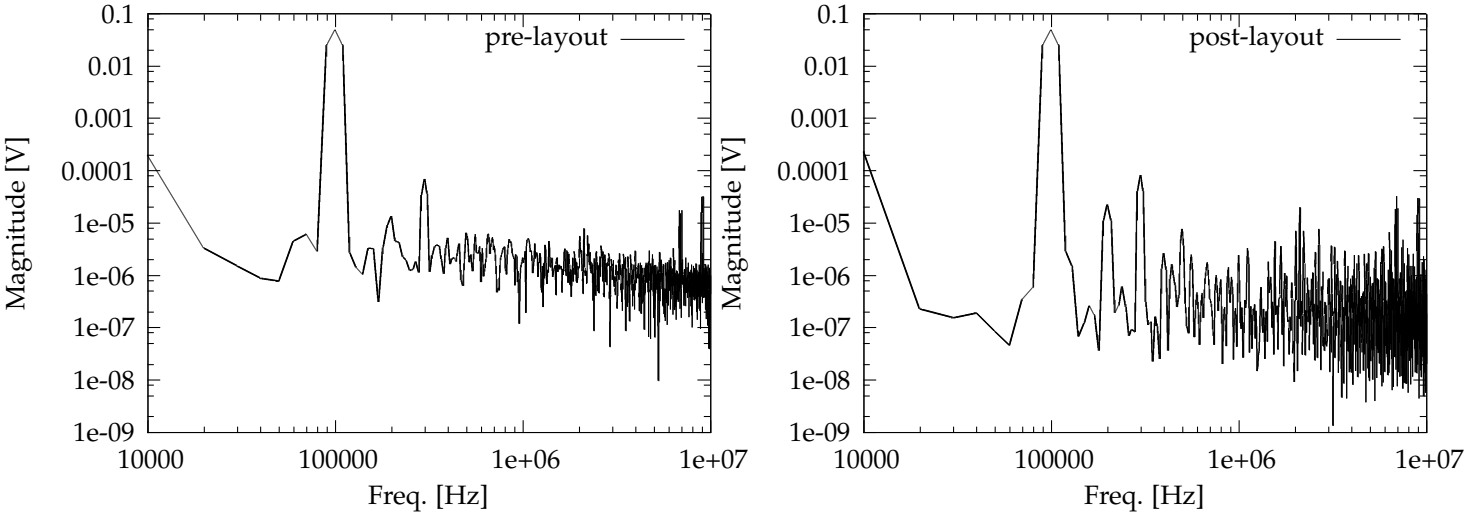


Figure 9: Spectrum of V_{out} at $V_{in} = 150\,\text{mV}$, which is the worst case SNDR for post-layout.

capacitor for C_1 and two for C_2, and with an extra dummy capacitor we could have realized the capacitors with a common-centroid layout with the four unit-sized capacitors. This would have increased the matching, but also increased the area. Four 600 fF capacitors has size of approx $4(17\mu\text{m} \times 17\mu\text{m}) = 1156\mu\text{m}^2$, nine 200 fF capacitors has size of approx $9(10\mu\text{m} \times 10\mu\text{m}) = 900\mu\text{m}^2$.

4.2 Comparison of specifications, pre- and post-layout results

Specifications	pre-layout	post-layout
In-band attenuation: < 3 dB	−2.099 dB	−2.150 dB
Dynamic range: > 8 bits	8.08 bits	8.74 bits
Settling time: < 19.5 ns	13.95 ns	n/a
Power usage: n/a	25.00 µW	18.75 µW

Settling time

The settling time for the pre-layout is within specifications. We assumed that the settling time would hold for post-layout as well. Furthermore, simulating just one switch and one of the capacitors would be difficult because we would have to redesign the layout for just this one test, also we would ignore a great deal of the parasitics and therefore the results would not be very accurate.

Power usage

We did not expect the power usage to be so much lower for the post layout. We are unsure why this happened. It could be because the layout introduced so many parasitic capacitances which smoothed out the signal, thus drawing less power from the source, we have included post- and pre-layout plots of the VDD where sharper transitions of the current and more spikes

in the current can be seen for the pre-layout simulation. Fig. 15 comparing pre- and post-layout power usage is included in appendix A.

Dynamic range and spectrum

The measured spectrum looked as expected with a much greater amount of high frequency noise caused by the added parasitics from the layout. Although we tried to separate the analog and digital part we could have improved the SNR greatly by separating analog and digital power supplies and grounds. The shared ground introduces a great deal of noise to the analog circuit because of digital switching in the clock circuit, especially since the clock circuit has so many inverters (26 in total). It was expected that the SNDR performance of the post-circuit would be limited by noise more than distortion. As is, we did not expect the post-layout simulation to yield better results for SNDR, which it did for lower input ranges, as the maximum result for SNDR was at 60mV for pre- and 30 mV for post-layout. We plotted both of the spectrums at 150 mV, we can clearly see that the post-layout circuit preformance is most limited by the harmonics while the pre-layout is limited by noise. Our circuit met the specs and the performance can therefore be said to be satisfactory.

Frequency response

It was expected that the frequency response would be worse for post-layout. The difference we see for the in-band attenuation for post- and pre-layout can be considered marginal, as it is about 0.05dB difference. The same can be said about the phase performance. Since the frequency response is well within the specs we could also allow for greater mismatch of the capacitors and therefore make the design less complicated.

We can see from the results that our circuit meets both the dynamic range and attenuation requirements. The bandwidth of the circuit is greater than what was required because of the higher chose clock frequency which also was the cause of the average results of the dynamic range performance of our circuit. We can see that our circuit has the frequency response corresponding to a first order system

4.3 Improvements

There are several improvements that could be made to our circuit. We could have separated analog and digital ground, because digital circuits produce a lot of noise that interferes with the analog parts. We could make the circuit slightly bigger to make room for more vias which would give us a higher yield and less resistance in wires. The increase in area would not be that great because the capacitors are so much larger than the rest of the circuit. The clock frequency we used could probably be reduced since we used such a small C2, this would probably give us a better dynamic range and use less power. If we had been more careful in our choice of C1 to C2 ratio, we could made the capacitor area smaller. Our design needed 7 unit capacitors + 2 dummies, but if we had made C2 twice the size of C1 and C1 unit size, we would only have needed 3 units + 2 dummies. To reduce charge injection we could modify the clock generator so that clk1' is off when clk1 turns off. The charge from the input switches will then flow to V_in instead of into C1 because of the high impedance that is produced. To reduce power usage we could have tried using smaller smaller PMOS switches. This would reduce the power usage and area of the circuit, and increase the settling time. However we have a pretty good margin on the settling time and could afford to increase it inorder to reduce power usage.

Bibliography

[1] Tony Chan Carusone, David Johns, Kenneth Martin *Analog integrated circuit design*. John Wiley & Sons, Inc. 2nd Edition, 2012.

5 Appendix A

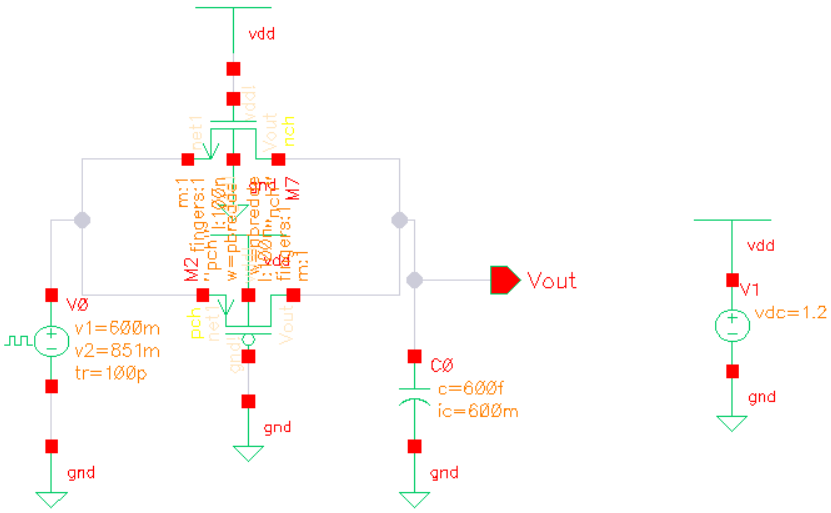


Figure 10: Test-bench used for Montecarlo simulation of CMOS switch to find settling time.

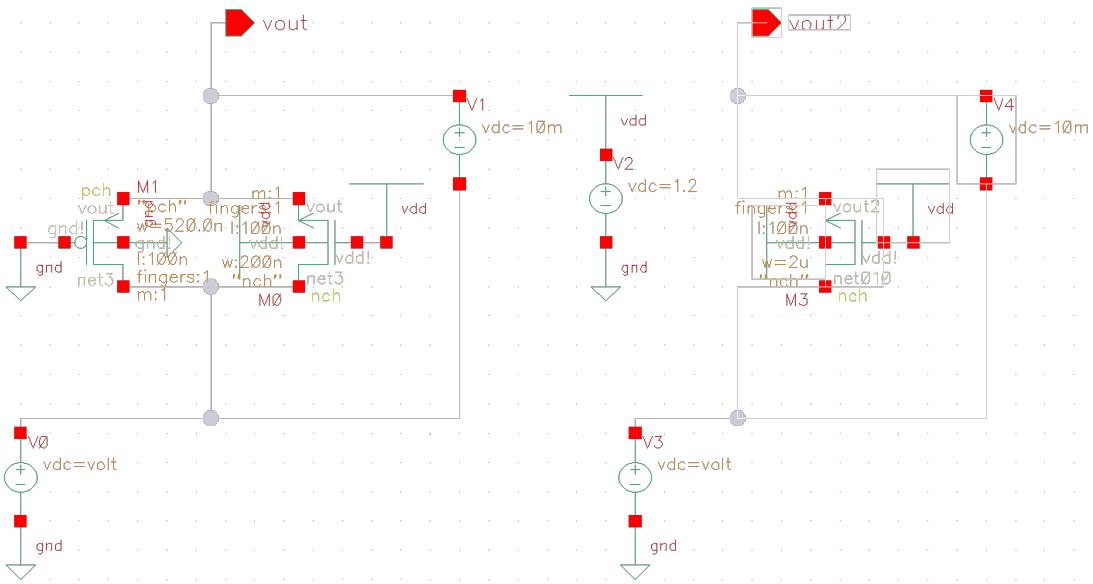


Figure 11: Test-bench used for Montecarlo simulation of CMOS switch to find R_{on}.

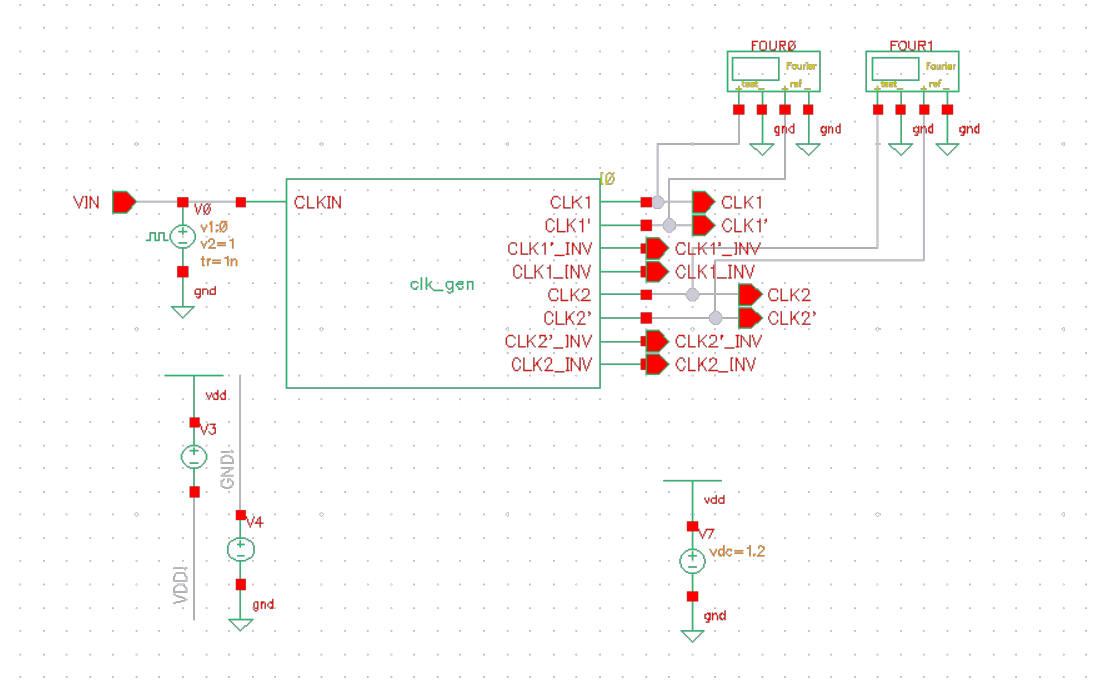


Figure 12: Test-bench used for testing the clock generator.

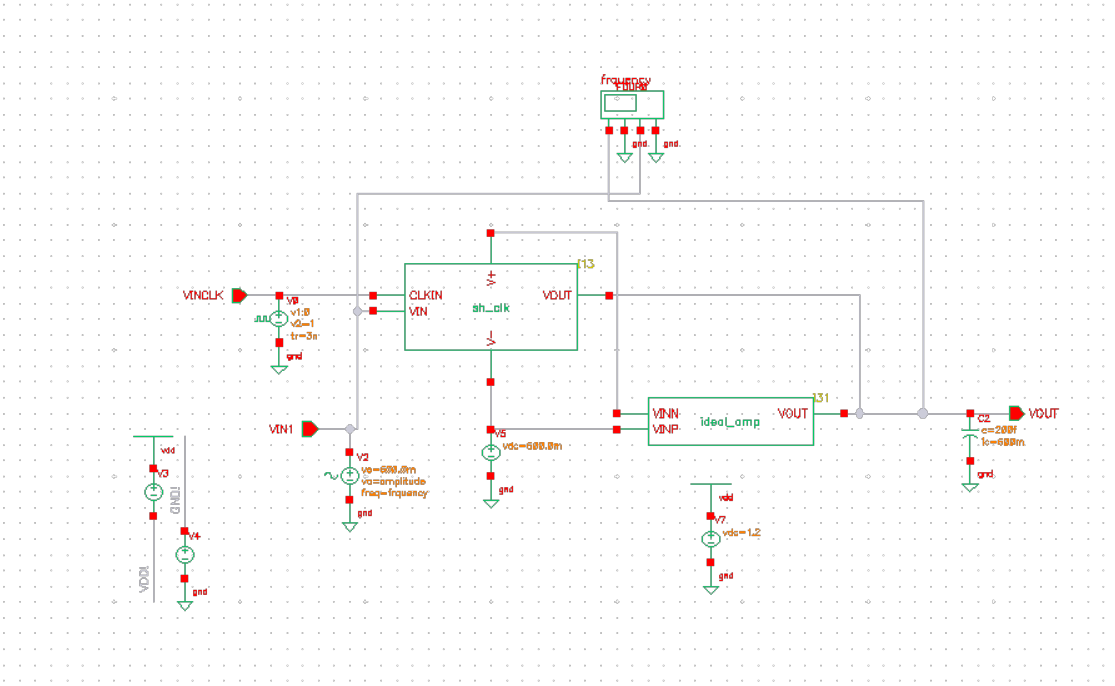


Figure 13: Test-bench used for testing the sample-and-hold.

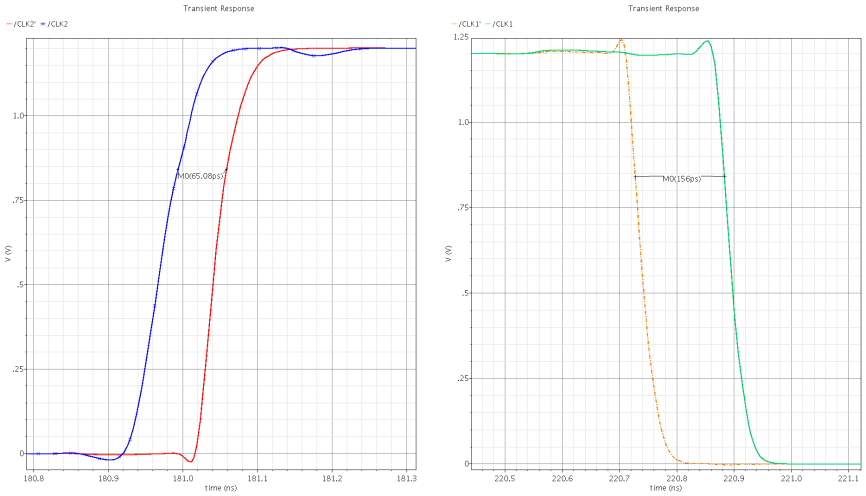


Figure 14: Delay between the clocks clk1, clk1' and clk2, clk2'

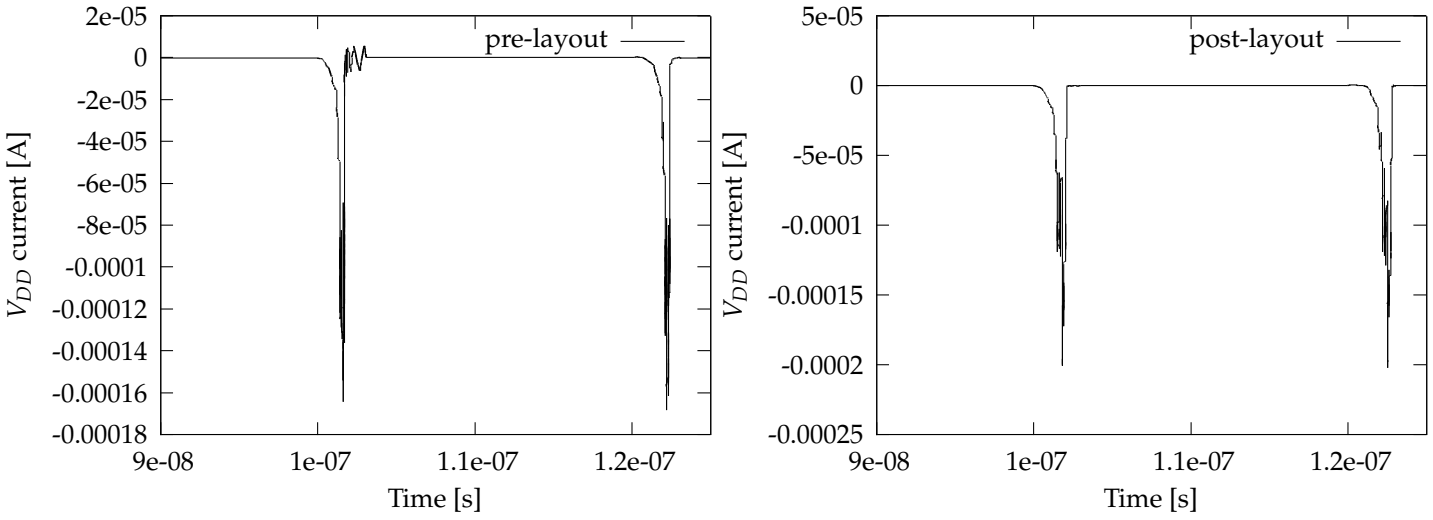


Figure 15: Comparison between pre- and post-layout transient simulation of VDD.

6 Appendix B

```
sndri = 0;

%the data matrix
data = dftmatrix;
dim = size(data);

tmp = 0; k = 1;
bits = 0;
amp = linspace(10e-3, 150e-3, dim(2)-1);
hpwr = zeros(dim(2)-1, 1);

%find index of 100kHz or find the maximum value (dominant freq.)
[x, y] = find(data==1e5);
if(isempty(x))
[x, y] = find(data==max(data(:, 2)));
end

for i = 2:dim(2)
k =1;
sndri(i-1) = data(x-1, i)^2 + data(x+1, i)^2 + data(x, i)^2;
for j = [2:x-2,x+2:dim(1)]
hpwr(i-1) = hpwr(i-1) + data(j, i)^2;
tmp(k, i-1) = data(j, i)^2;
k = k + 1;
end

sndr(i-1) = 10*log10(sndri(i-1)/hpwr(i-1));
bits(i-1) = (sndr(i-1) + 1.79)/6.02;
end
```