INF3410 - ANALOG MICROELECTRONICS

LAB 2

MOS AMPLIFIERS

Eino Juhani Oltedal(einojo)
einojo@student.matnat.uio.no

Maris Tali(maristal)
maristal@student.matnat.uio.no

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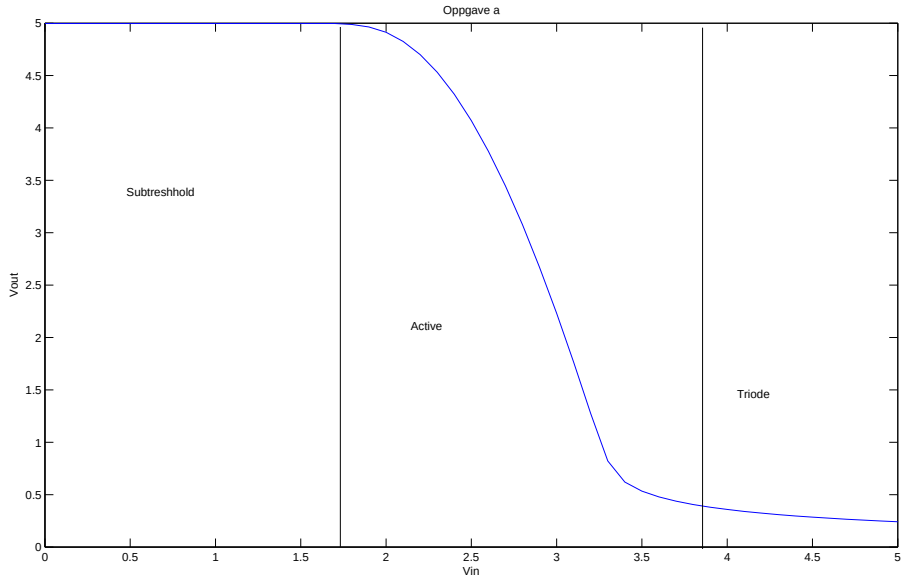
Question a



Figur 1: Output voltage as a function of input voltage of a NMOS with pull-up resistor, operation regions identified on plot.

The NMOS transistor is in subtreshold region region when

$$V_{GS} < V_t \tag{1}$$

The NMOS transistor is in triode region region when

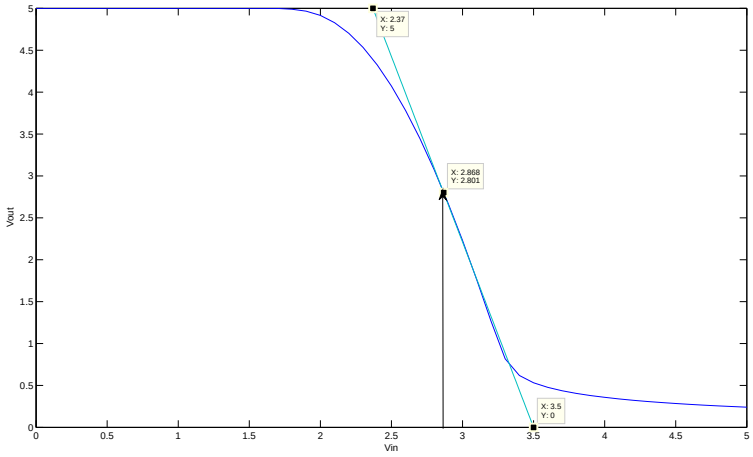
$$V_{GS} > V_t, V_{DS} <= V_{eff} \tag{2}$$

The NMOS transistor is in active region when

$$V_{GS} > V_t, V_{DS} >= V_{eff} \tag{3}$$

The V_t of the transistor is approximated to $1.7V$.

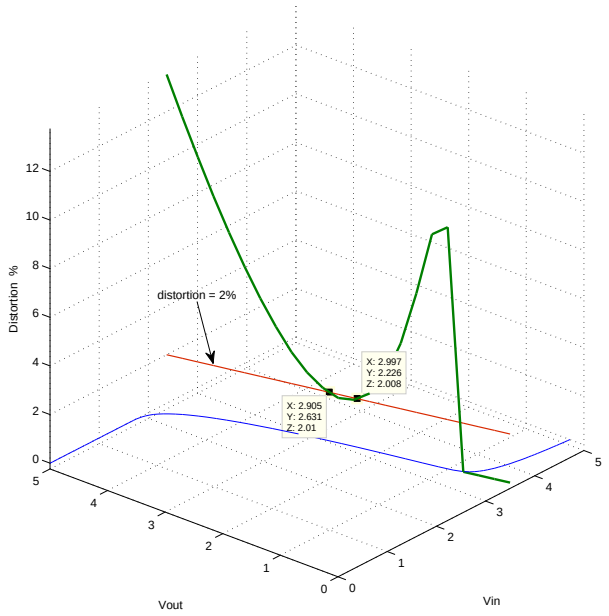
Question b



Figur 2: Linear approximation around the operating point plotted with data from figure

$A_V = \frac{\Delta Y}{\Delta X} = \frac{5-0}{2.37-3.5} = \frac{5}{-1.13} = -4.43$ Which means that the estimated gain of the circuit is 4.43.

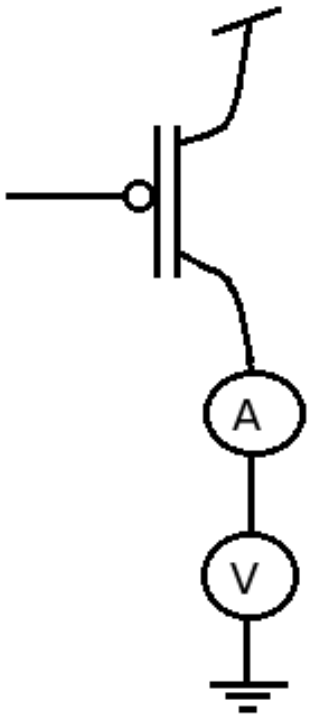
Question c



Figur 3: Distortion between the measured an the approximate trace.

The distortion between the approximated signal and the simulated data is only less than 2% between $Vin = [2,905V; 2.997V]$ which means that the amplifier only has a linear amplification region of $0.092V$. We can cocnclude with that the amplifiers linear response is quite limited.Still, the amplifier is reasonably linear in the region $2.5Vto3.1V$.

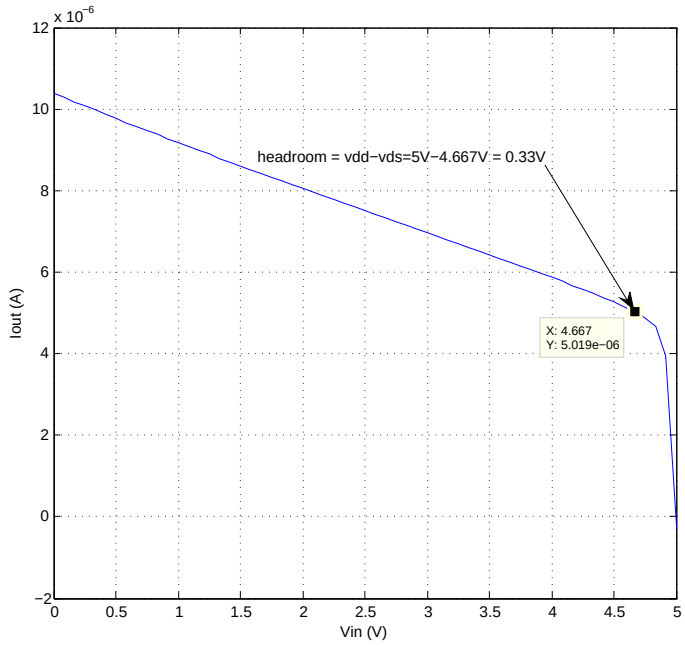
Question d



Figur 4: Schematic of biased PMOS used in question d and e.

We selected a biasing voltage of 3.93 V had a drain source voltage of 2 V this gave us a drain current of 10μA. To determine r_{ds2} we plotted the drain current against the drain source voltage in figure **??**, and found the slope of the linear (active) region. This gave the result $r_{ds2} = 880.4\,\text{k}\Omega$. The current was measured by connection a amepere meter to the drain of the PMOS in series with a voltage source which was connected to ground as shown in figure 4.

Question e



Figur 5: Drain current plotted against drain source voltage with headroom marked

A headroom voltage of $V_{dd} - V_{ds} = 0.33\,\text{V}$ is required so that the PMOS is in the active region.

Question f

Using the forumla of I_D we can find $\mu_n C_{ox} \frac{W}{L}$ by using the the biasing voltage found in question d $V_{GS} = V_{bias} = 3.93\,\text{V}$, the drain current $I_D = 10\mu\text{A}$, the drain source voltage $V_{DS} = 2\,\text{V}$, and $r_{ds} = 880.4\text{k}\Omega$. We used the threshold voltage found in last lab $V_{tn} = 1.8\text{V}$

$$V_{eff} = V_{GS} - Vtn = 3.93\text{V} - 1.8\text{V} = 2.13\text{V} \tag{4}$$

Since $(V_{GS} > Vtn, V_{DS} \leq V_{eff}$ the transistor is in the triode region. Therfore I_D becomes:

$$\begin{aligned} I_d &= \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_{tn})V_{DS} - \frac{V_{DS}^2}{2}] \\ \mu_n C_{ox} \frac{W}{L} &= \frac{I_D}{[(V_{GS} - V_{tn})V_{DS} - \frac{V_{DS}^2}{2}]} \\ \mu_n C_{ox} \frac{W}{L} &= \frac{10 * 10^{-6}\text{A}}{[(3.93\text{V} - 1.8\text{V})2\text{V} - \frac{4\text{V}}{2}]} \\ \mu_n C_{ox} \frac{W}{L} &= \frac{10 * 10^{-6}\text{A}}{[(2.13\text{V})2\text{V} - 2\text{V}]} \\ \mu_n C_{ox} \frac{W}{L} &= \frac{10 * 10^{-6}\text{A}}{[(2.26\text{V}]} \\ \mu_n C_{ox} \frac{W}{L} &= 4.43 * 10^{-6}\text{A/V} \end{aligned} \tag{5}$$

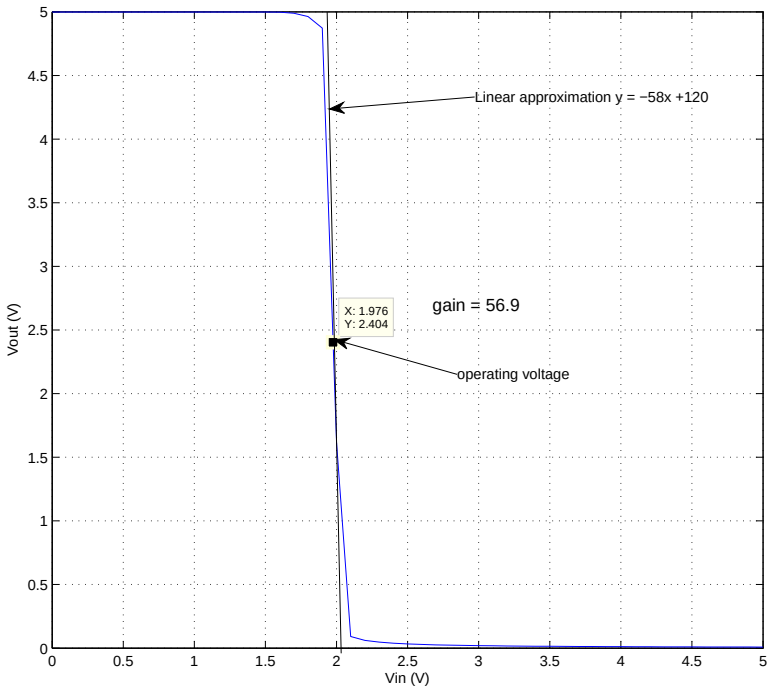
$\mu_n C_{ox} \frac{W}{L}$ can now be used to calculate g_m with $I_{bias} = 100\mu\text{A}$

$$\begin{aligned} g_m &= \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) \cdot I_{bias}} \\ g_m &= \sqrt{2 * 4.43 * 10^{-6} * 100 * 10^{-6}\text{A}} \\ g_m &= 2.97 * 10^{-5} \end{aligned} \tag{6}$$

Finally the gain can be calculated by $A_V = -g_m[r_{ds1}||r_{ds2}]$. We assume that the r_{ds} of the PMOS and NMOS are the same

$$\begin{aligned} r_{ds1}||r_{ds2} = r_{ds}||r_{ds} &= \frac{r_{ds}}{2} = \frac{880.4\text{k}\Omega}{2} = 440.2\text{k}\Omega \\ A_V &= -g_m r_{ds}) \\ A_V &= -13.1 \end{aligned} \tag{7}$$

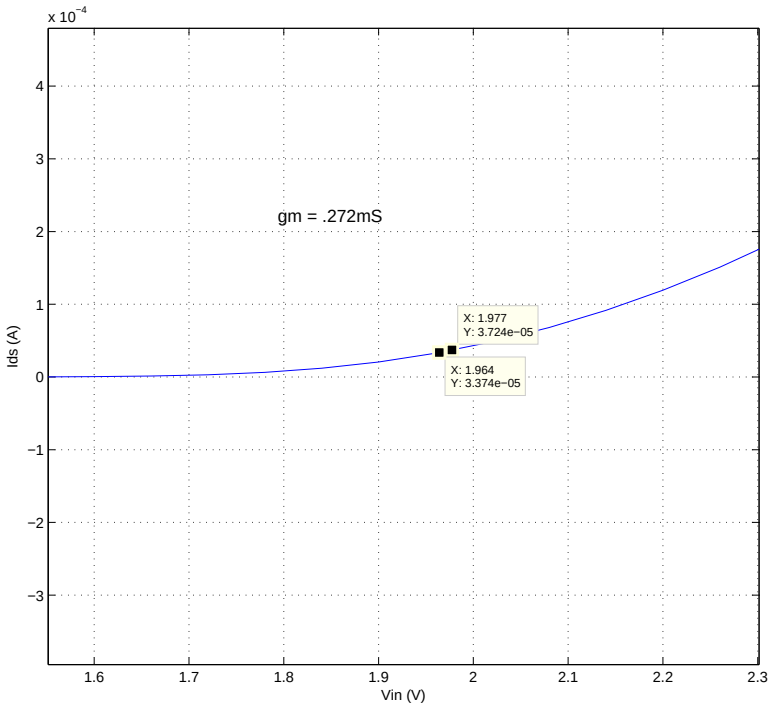
Question g



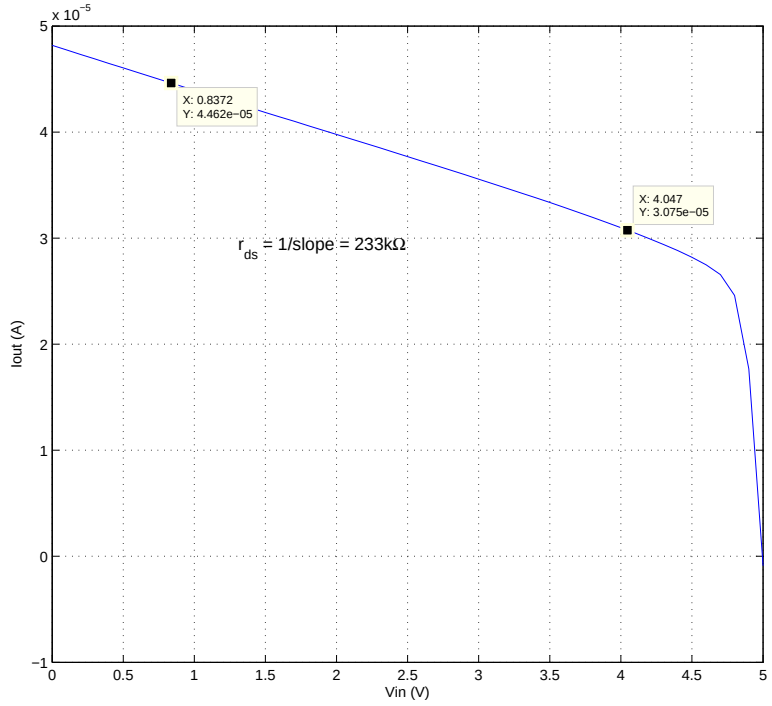
Figur 6: Output voltage plotted against input voltage with a linear approximation tangent to the operating voltage of 1.99V. $V_{bias} = 3.79\text{V}$ $I_{bias} = 48.0\mu\text{A}$

The gain of the amplifier is the slope of the linear approximate in figure 6 $A_V = 56.9$. The gain from the amplifier with passive load was 4.43, comparing the two we get $\frac{56.9}{4.43} = 12.8$. Which means the gain from the active load common source amplifier is 12.8 times greater than the gain from the passive load amplifier.

Question h



Figur 7: Drain current plotted against gate voltage (V_{in}). The $g_m = .272mS$ is the slope of the tanget at the operating voltage 1.99V. $V_{bias} = 3.79\text{V}$ $I_{bias} = 48.0\mu\text{A}$



Figur 8: Drain current plotted against drain source voltage ($V_{in} = V_{ds}$). $r_{ds} = 233\text{k}\Omega$ is $\frac{1}{slope}$ of the curve in the active region. $V_{bias} = 3.79\text{V}$ $I_{bias} = 48.0\mu\text{A}$

Using the out put resistance from the NMOS and PMOS transistor, and the g_m of the NMOS we can calculate the gain of the amplifier accurately. $r_{ds1} = 880.4\text{k}\Omega$ $r_{ds2} = 233\text{k}\Omega$

$$\begin{aligned} A_V &= gm(r_{ds1}||r_{ds2}) \\ A_V &= gm\left(\frac{880.4\text{k}\Omega \cdot 233\text{k}\Omega}{880.4\text{k}\Omega + 233\text{k}\Omega}\right) \\ A_V &= gm\left(\frac{880.4\text{k}\Omega \cdot 233\text{k}\Omega}{880.4\text{k}\Omega + 233\text{k}\Omega}\right) \\ A_V &= gm(184.2\text{k}\Omega) \\ A_V &= 0.272 * 10^{-3}\text{mS}(184.2\text{k}\Omega) \\ A_V &= 50.1 \end{aligned} \tag{8}$$

This gain approximate is really close to the approximate from question g. The difference $A_{questioG} - A_{questioH} = 56.9 - 50.1 = 6.8$ is small, which means both are good ways to approximate the gain. This gain approximate is very different from the approximate found in question f. Some of that difference can be explained, by the fact that a biasing current of $100\mu\text{A}$ was used in question j while a biasing current of $48\mu\text{A}$ was used in questions g and h. However this in not enough to explain the large difference $A_{questionH} - A_{questionJ} =$

$50.1 - 13.1 = 37$. In question j we assumed that the g_m and r_ds of the PMOS was equal to the g_m and r_ds of the NMOS, this can not be true since we got such a large difference, therefore making that assumption is not a good way of approximating the gain of the active load common source amplifier.

Question i

We can assume that the two NMOS transistors with input V_+ and V_- have the same g_m. The current through the NMOS with V_+ on the gate should be $\frac{V_+}{r_{s1}}$ where $r_{s1} = 1/g_m$ thus $I_{d1} = V_+ \cdot g_m$. The current through the left NMOS is the same as the current through the left PMOS, therfore $I_{d1} = I_{s1}$. The PMOS transistors form a current mirror so the same current passes through both transistors, thus $I_{s1} = I_{s2}$. The current through the right NMOS is calculated the same way as the current through the left NMOS, therefore $I_{d2} = V_- \cdot g_m$. Since there is a split in the wire here $I_{s2} = I_{out} + I_{d2}$ the current out must be

$$\begin{aligned} I_{out} &= I_{s2} - I_{d2} \\ I_{out} &= I_{s1} - I_{d2} \\ I_{out} &= I_{d1} - I_{d2} \\ I_{out} &= V_+ \cdot g_m - V_- \cdot g_m \\ I_{out} &= (V_+ - V_-) g_m \\ I_{out} &= V_{diff} g_m \end{aligned} \tag{9}$$

The output current in strong inversion is given by $I_{out} = V_{diff} g_m$.

Question j

In weak inversion the current through the left NMOS is given by

$$I_1 = I_0 \exp\left(\frac{V_+ - nv}{nU_t}\right) \tag{10}$$

the current through the right NMOS is given by

$$I_1 = I_0 \exp\left(\frac{V_- - nv}{nU_t}\right) \tag{11}$$

and the current through the tail is given by

$$\begin{aligned} I_b &= I_1 + I_2 \\ I_b &= I_0 \exp\left(-\frac{v}{U_T}\right)\left(\exp\left(\frac{V_-}{nU_t}\right) + \exp\left(\frac{V_+}{nU_t}\right)\right) \end{aligned} \tag{12}$$

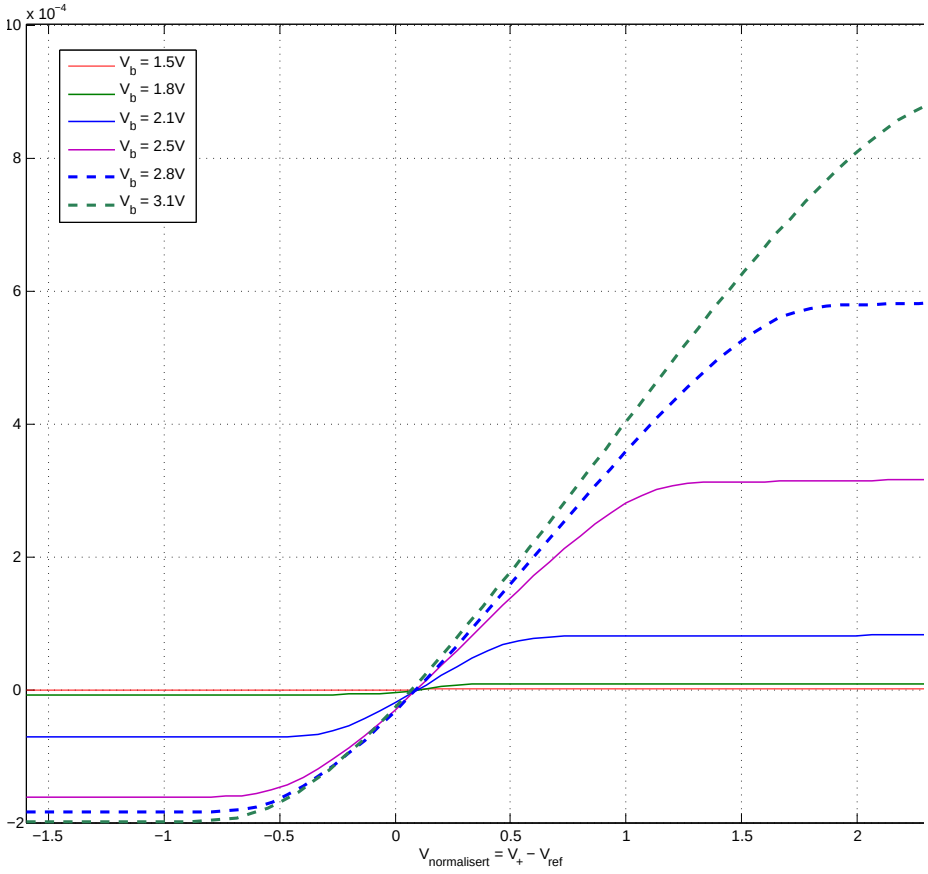
This gives

$$\begin{aligned}
\exp\left(-\frac{v}{U_T}\right) &= \frac{I_b}{I_0}\frac{1}{\left(\exp\left(\frac{V_-}{nU_t}\right)+\exp\left(\frac{V_+}{nU_t}\right)\right)} \\
I_1 &= I_b\frac{\exp\left(\frac{V_+}{nU_T}\right)}{\left(\exp\left(\frac{V_-}{nU_t}\right)+\exp\left(\frac{V_+}{nU_t}\right)\right)} \\
I_2 &= I_b\frac{\exp\left(\frac{V_-}{nU_T}\right)}{\left(\exp\left(\frac{V_-}{nU_t}\right)+\exp\left(\frac{V_+}{nU_t}\right)\right)} \\
I_{1(2)} &= \frac{I_b}{1+\exp\left(\frac{V_+-V_-}{nU_t}\right)} \\
I_{out} &= I_1 - I_2 = I_b\tanh\left(\frac{V_+ - V_-}{2nU_T}\right) \\
I_{out} &= I_1 - I_2 = I_b\tanh\left(\frac{V_{diff}}{2nU_T}\right)
\end{aligned} \tag{13}$$

The output current in weak inversion is given by $I_{out} = I_1 - I_2 = I_b \tanh\left(\frac{V_{diff}}{2nU_T}\right)$.

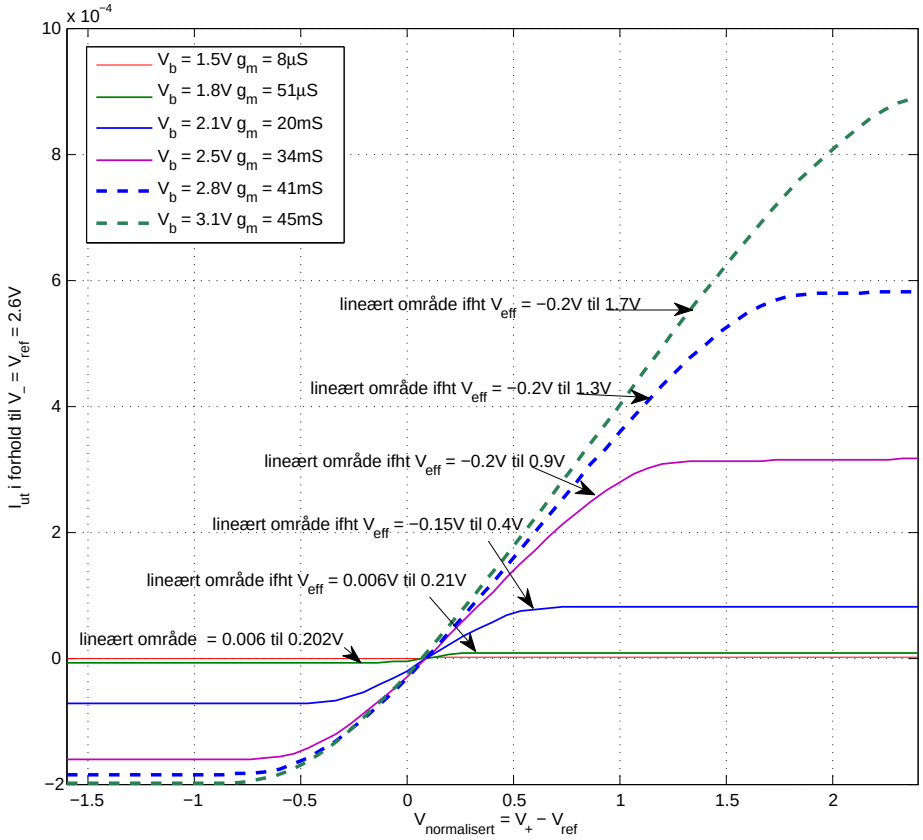
Question k

$V_{ref} = V_-$ was chosen as 2.6V and the 6 tail currents are $V_{bias} = 3.1V, 2.8V, 2.5V, 2.1V, 1.8V$ and $1.5V$. The threshhold voltage is approx $1.8V$ so the two last tail currents describe the transistor in weak inversion. The X-axis of the plot is normalized to $V_{normalisert} = V_+ - V_{ref}$ so the point of maximum gain is in the origo.



Figur 9: I_{out} in reference to V_{ref} plotted agains the normalised V_{in}

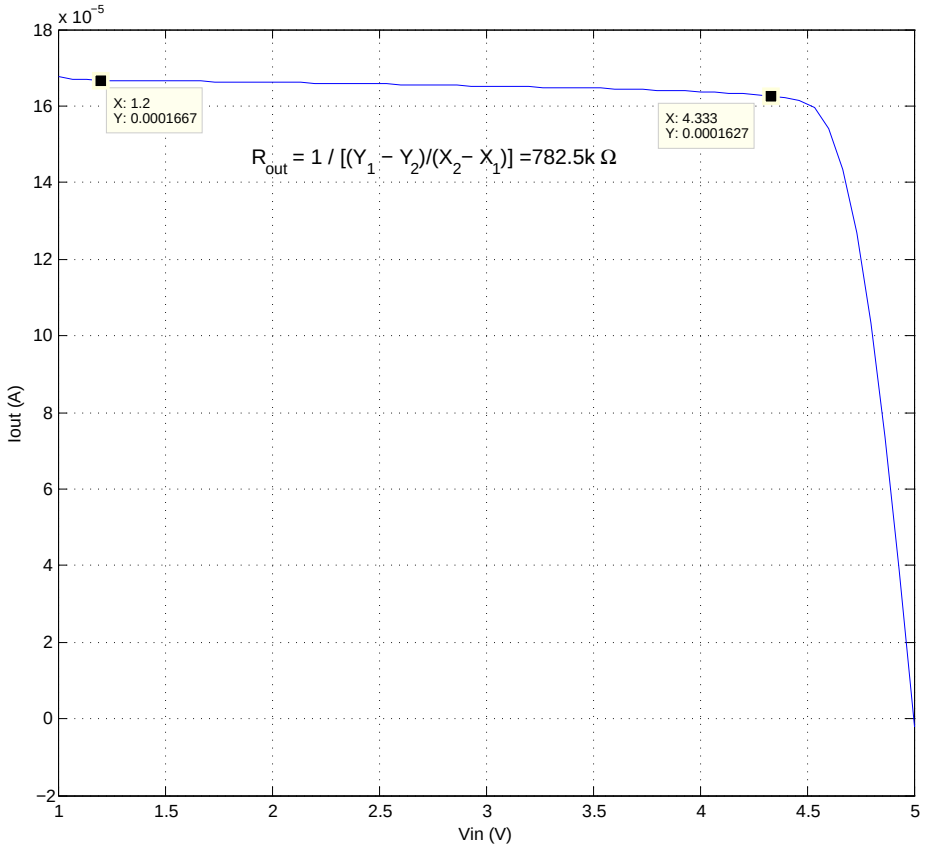
The linear region is marked for each current in relation to $V_{ref} = 2.6V$ and gm is found by calculating the maximum slope for each tail current. It can be seen from the plot that Gm is very small in weak inversion compared to the strong inversion Gms.



Figur 10: I_{out} in reference to V_{ref} plotted agains the normalised V_{in} with linear regions and gm marked in the plot

Question 1

A voltage difference of $V_+ - V_- = 2.7V - 2.5V = 0.2V$ was applied to the amplifier, V_{bias} was set to $2.5V$ and the output voltage was swept from $1V$ to $5V$. The output resistance was calculated as $R_{out} = \frac{1}{slope}$ and was found to be $782.5k\Omega$.



Figur 11: Output current plotted against the swept output voltage, R_{out} marked on the plot

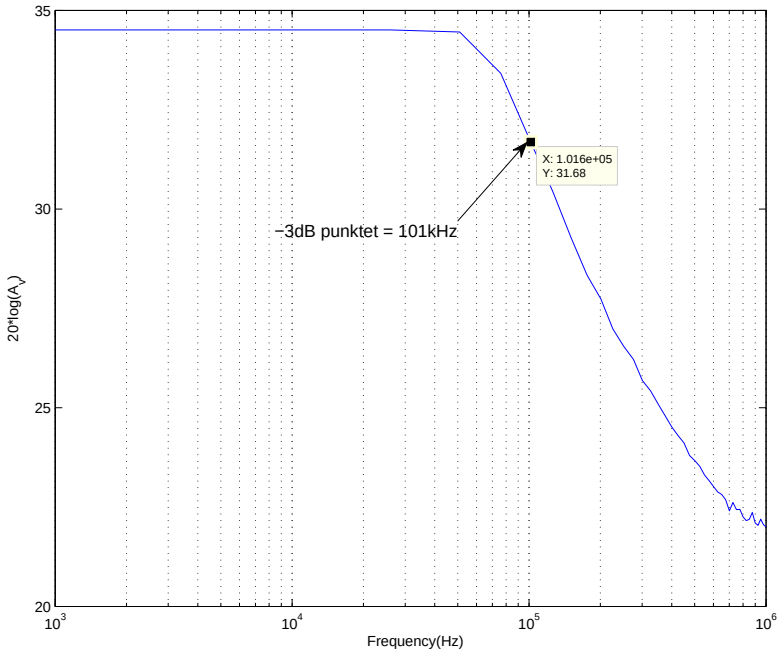
The gain of the amplifier for the 6 tail currents:

$$\begin{aligned} A_V &= R_{out} \cdot G_m \\ V_b = 1.5V, A_{V1} &= 782.5k\Omega \cdot 8\mu S = 0.6 \\ V_b = 1.8V, A_{V2} &= 782.5k\Omega \cdot 51\mu S = 40 \\ V_b = 2.1V, A_{V3} &= 782.5k\Omega \cdot 20mSA = 161 \\ V_b = 2.5V, A_{V4} &= 782.5k\Omega \cdot 34mSA = 269 \\ V_b = 2.8V, A_{V5} &= 782.5k\Omega \cdot 41mSA = 321 \\ V_b = 3.1V, A_{V6} &= 782.5k\Omega \cdot 45mSA = 358 \end{aligned} \tag{14}$$

These results are about 6 times larger than the measured A_v is.

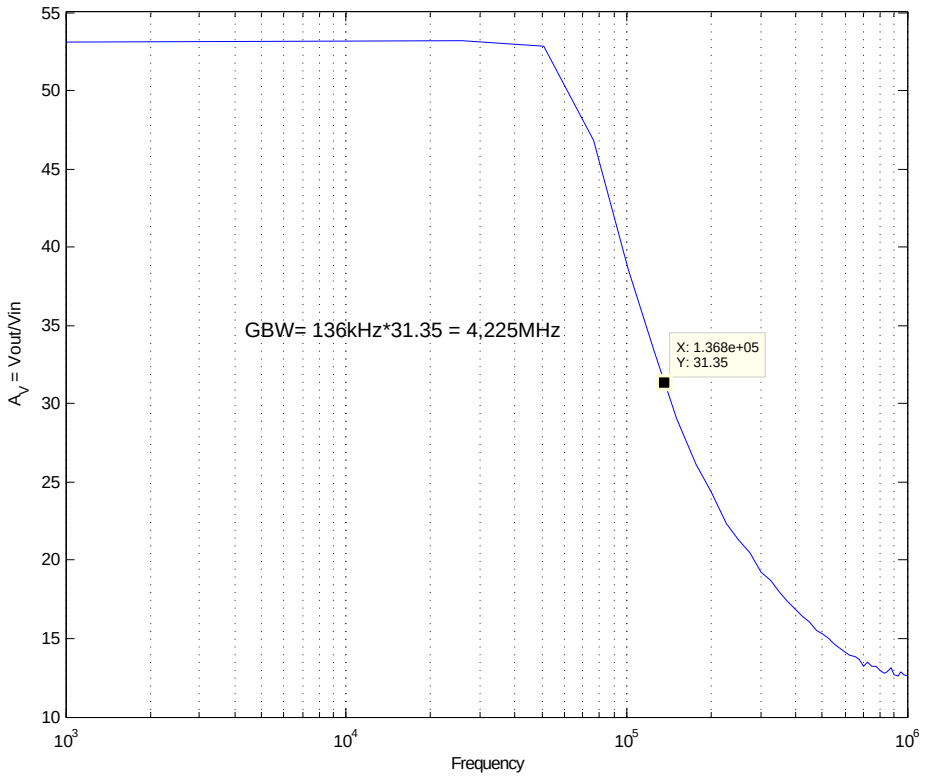
Question m

A tail current of 2.5V was used to bias the tansistor in strong inversion and an AC voltage of 100mV_{PP} in reference to the V_{bias} of 2.5v. The $-3dB$ point is marked on the plot and was found to be 101kHz, The X-axis is logarithmic and the Y-axis is the amplification $Av = 20 \cdot \log(V_{out}/V_{in})$ in dB.



Figur 12: Amplification in dB plotted against a logarithmic frequency axis (Bode plot)

The GBW can be found by taking the product of the aplification $A_V = V_{out}/V_{in}$ and the corresponding frequency, in our case $GBW = 136kHz \cdot 31.35 = 4.22MHz$ whic is a reasonable result.



Figur 13: Amplification plotted against a logarithmic frequency axis