INF3410 - ANALOG MICROELECTRONICS

LAB 1

MOS TRANSISTOR - MODEL AND REALITY

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Group: 1
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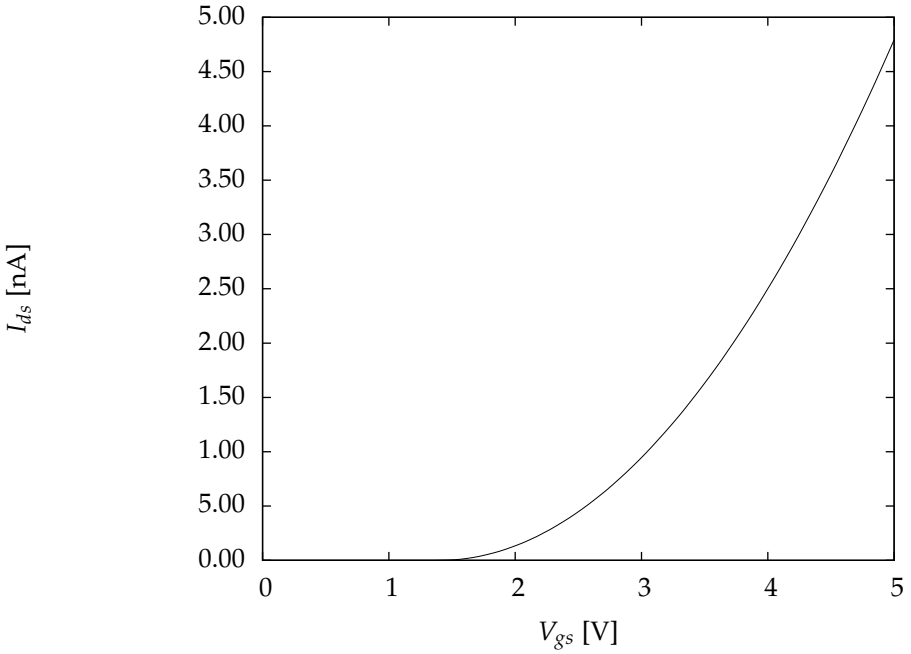
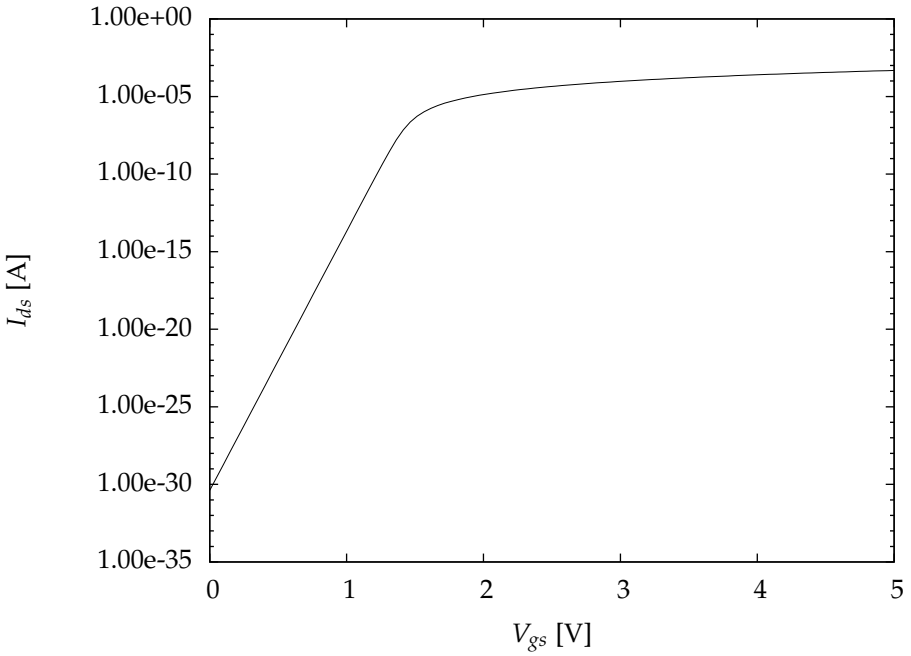
Question a



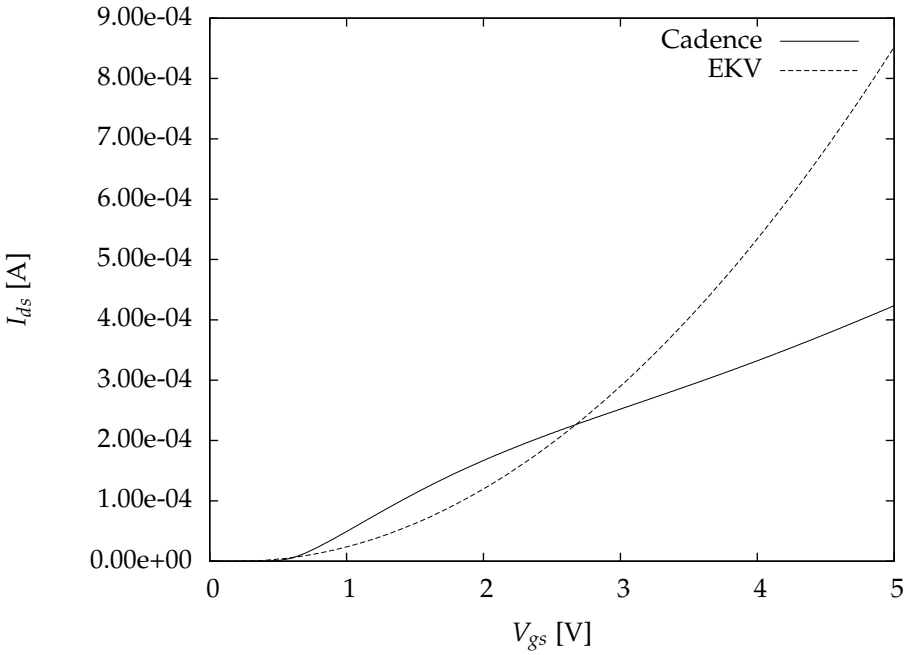
Figur 1: Drain-source current as a function of the gate-source voltage of a NMOS transistor in the active region (linear plot).



Figur 2: Drain-source current as a function of the gate-source voltage of a NMOS transistor in the active region (logarithmic y-axis plot).

I figur 1 settes spenningene 3V, 2V, og 5V som input. Da blir $Sum\_ut = 10V$, siden $3V + 2V + 5V = 10V$. Altså fungerer summasjonskretsen.

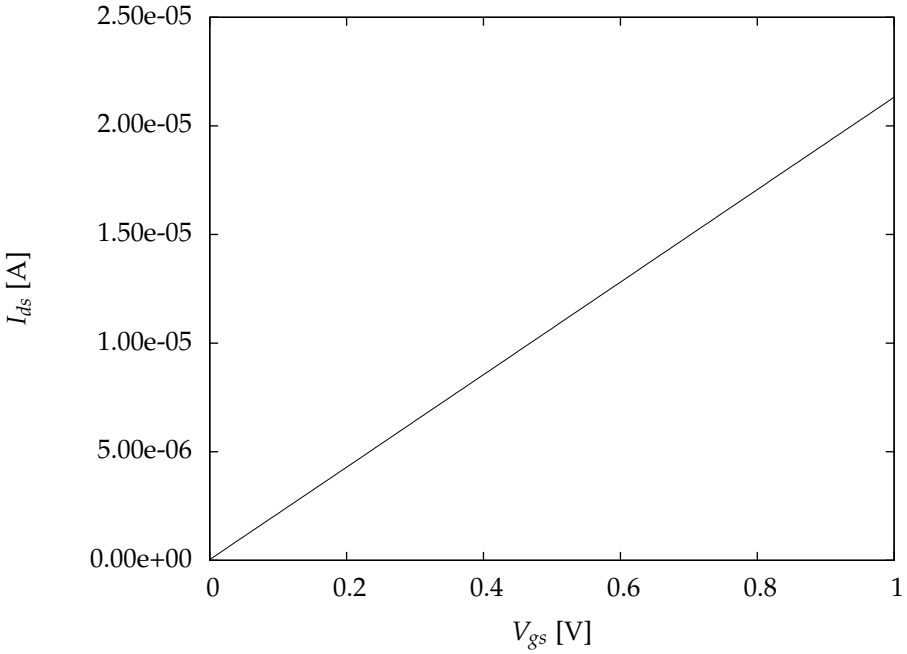
Question b



Figur 3: Drain-source current as a function of the gate-source voltage of a NMOS transistor in the active region (logarithmic y-axis plot).

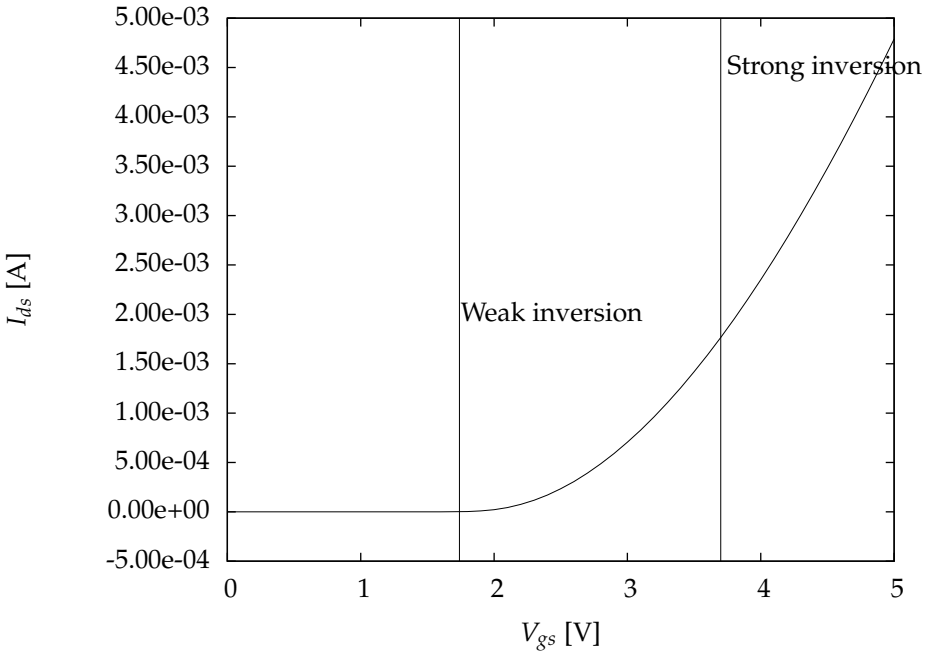
In figur 3 we tried to adjust the EKV parameter to fit the CADENCE curve, we did this by adjusting the threshold voltage from 0.7V to 0.2V. We could only get the beginning of the curve to look similar because the model we used in matalb does not include mobility degradation.

Question c



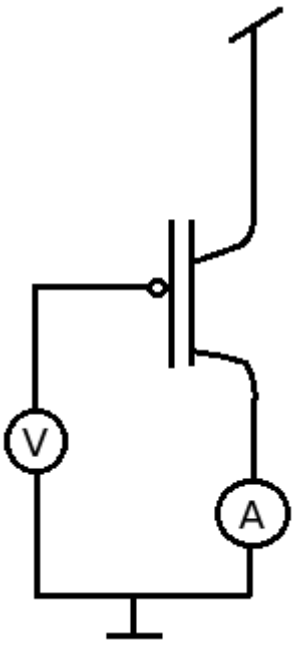
Figur 4: Current through a $50k\Omega$ resistor as a function of applied voltage.

Question d



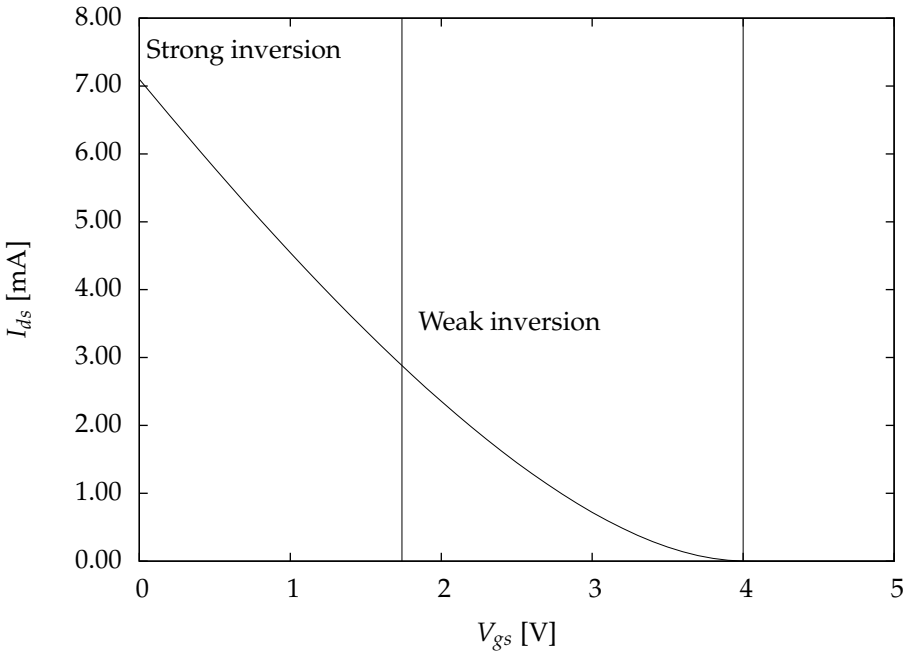
Figur 5: Drain-source current as a fuction of the gate-source voltage in a NMOS transistor.

Question e



Figur 6: PMOS transistor measuring setup.

Question f



Figur 7: Drain-source current as a fuction of the gate-source voltage in a PMOS transistor.

Question g

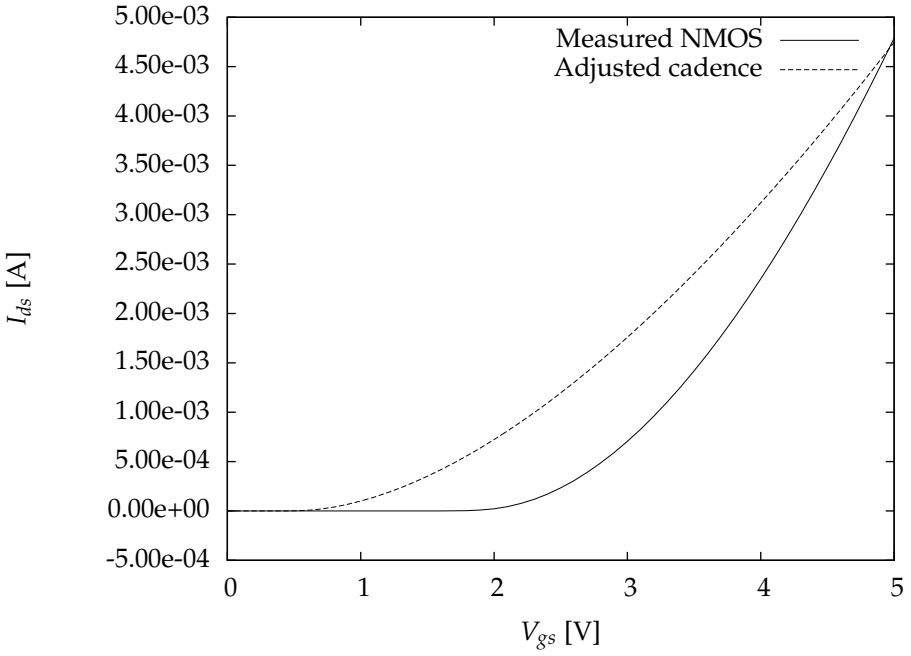
The PMOS is active when the gate voltage is low, while the NMOS is active when the gate voltage is high. There is also a difference in the drain source current. this may be because the PMOS conducts with holes, while the NMOS conducts with electrons in its respective channels. This means that the mobility of the NMOS will be 2-3 times the mobility of the PMOS.

Question h

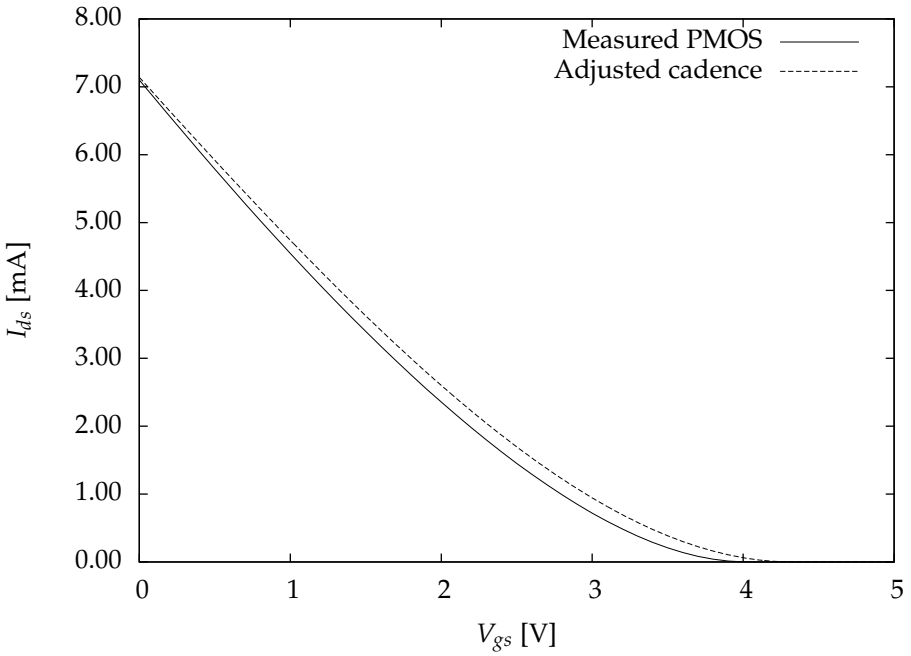
We changed the EKV parameters as follows: the V_t to 1.5V and I_s to 1μA.

Question i

Question j



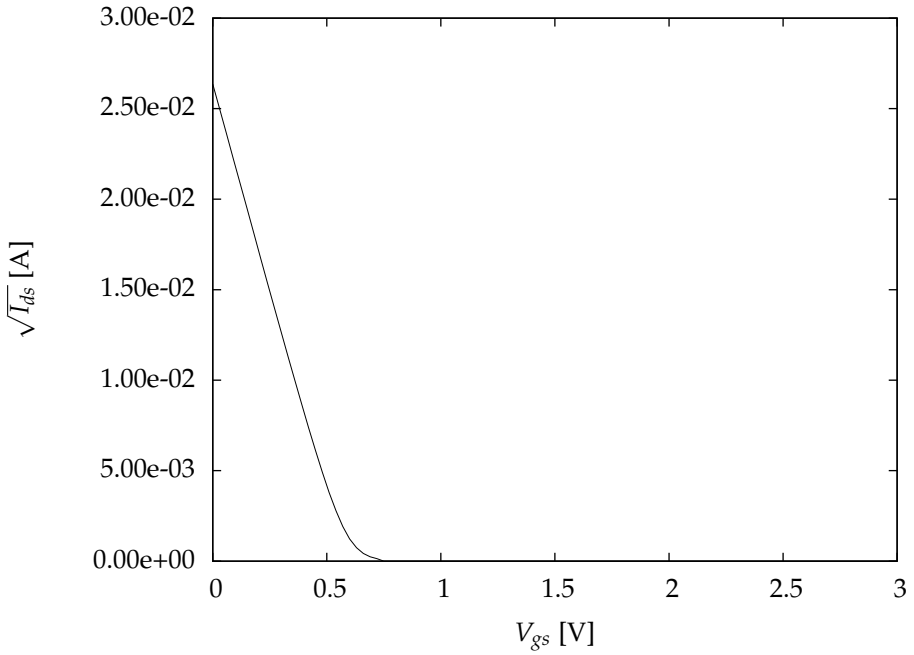
Figur 8: Drain-source current as a fuction of the gate-source voltage in a NMOS transistor and a cadence simulation with $width = 26\mu m$ $length = 5\mu m$.



Figur 9: Drain-source current as a fuction of the gate-source voltage in a PMOS transistor and a cadence simulation with $width = 124\mu m$ and $length = 5\mu m$.

By increasing the width and length of the transitors in the candence simulations of figures 8 and 9 the transistors did no go into mobility degradation. By increasing the width further I_{ds} was also increased. The Measured and simulated plots now look very similar. The simulation is a bit off in figure 8 because we did not adjust the threshold voltage.

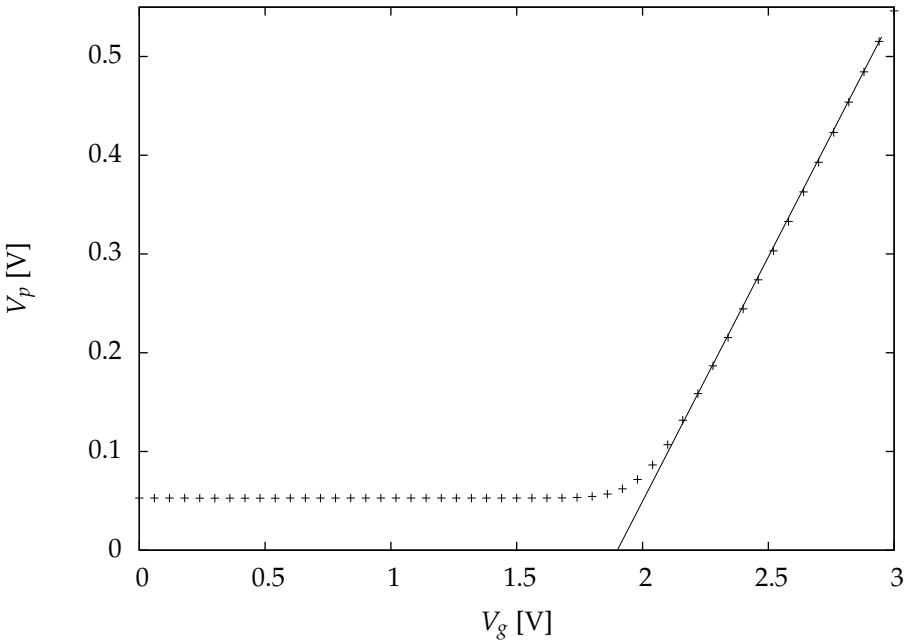
Question k



Figur 10: Drain-source current as a function of the gate-source voltage of a NMOS transistor in the active region (logarithmic y-axis plot).

$V_G = 3V$ V_S from 0V to 3V. $V_{DD} = 3.5V$

Question l



Figur 11: V_p as a function of the gate Voltage, with extrapolation of the linear region to determine the Zero-biased Threshold voltage.